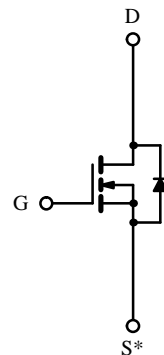
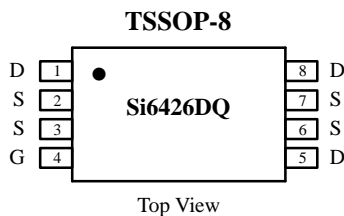


**N-Channel Enhancement-Mode MOSFET**

**Product Summary**

$V_{DS}$ (V)	$r_{DS(on)}$ ( $\Omega$ )	$I_D$ (A)
20	0.035 @ $V_{GS} = 4.5$ V	$\pm 5.4$
	0.04 @ $V_{GS} = 2.5$ V	$\pm 4.9$



\*Source Pins 2, 3, 6, and 7 must be tied common.

N-Channel MOSFET

**Absolute Maximum Ratings ( $T_A = 25^\circ\text{C}$  Unless Otherwise Noted)**

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	20	V
Gate-Source Voltage	$V_{GS}$	$\pm 8$	
Continuous Drain Current ( $T_J = 150^\circ\text{C}$ ) <sup>a</sup>	$I_D$	$T_A = 25^\circ\text{C}$	A
		$T_A = 70^\circ\text{C}$	
Pulsed Drain Current	$I_{DM}$	$\pm 30$	A
Continuous Source Current (Diode Conduction) <sup>a</sup>	$I_S$	1.25	
Maximum Power Dissipation <sup>a</sup>	$P_D$	$T_A = 25^\circ\text{C}$	W
		$T_A = 70^\circ\text{C}$	
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to 150	$^\circ\text{C}$

**Thermal Resistance Ratings**

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient <sup>a</sup>	$R_{thJA}$	83	$^\circ\text{C}/\text{W}$

Notes

a. Surface Mounted on FR4 Board,  $t \leq 10$  sec.

Subsequent updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #1807. A SPICE Model data sheet is available for this product (FaxBack document #5137).

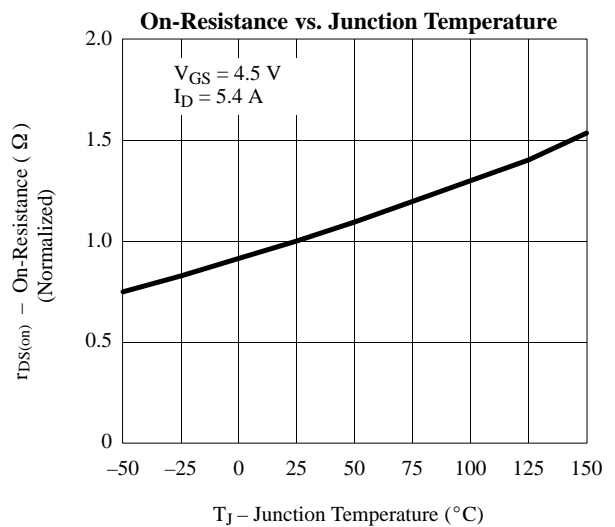
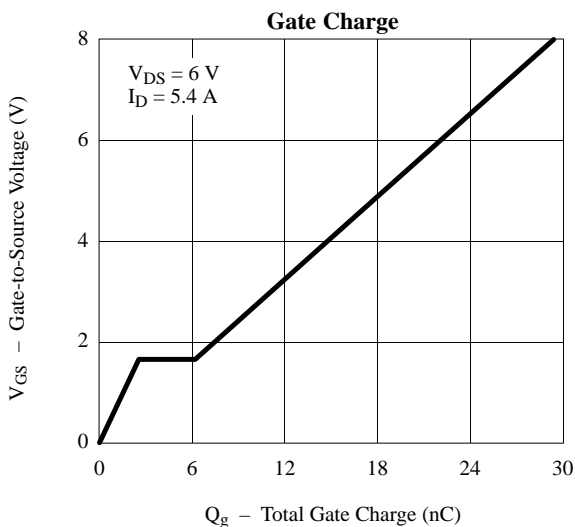
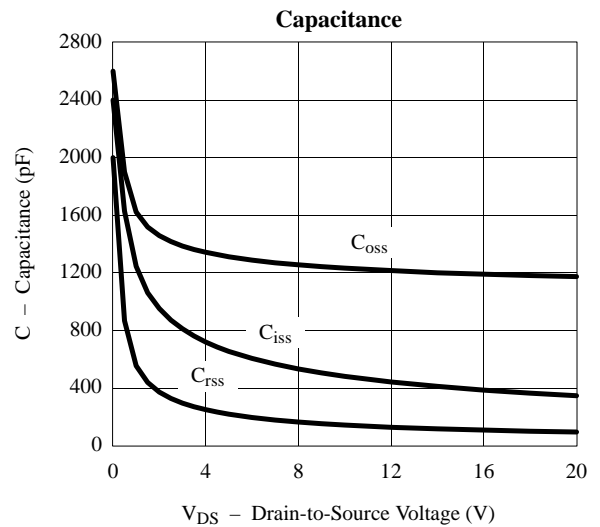
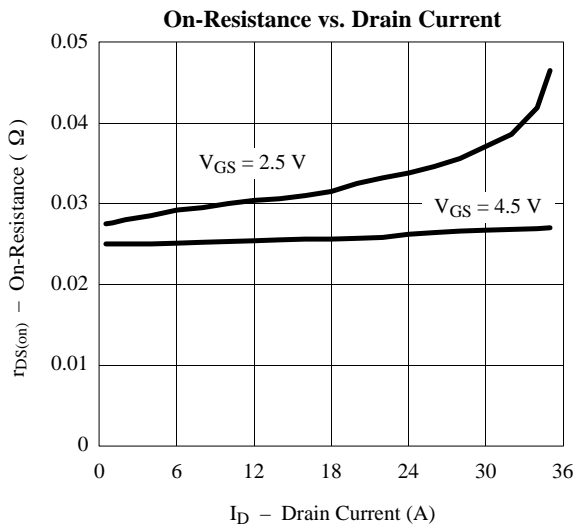
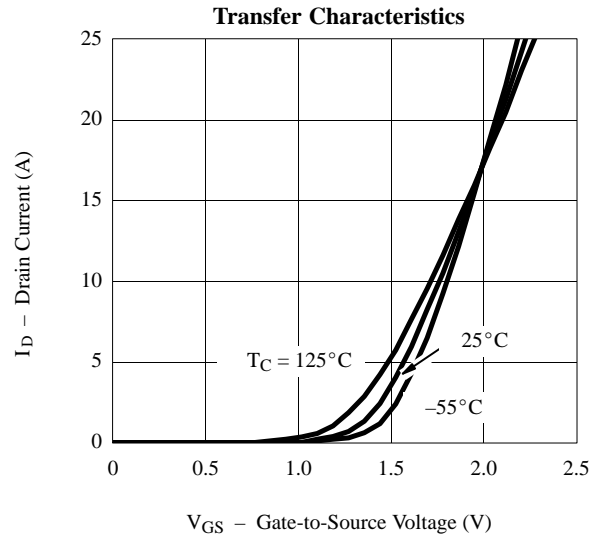
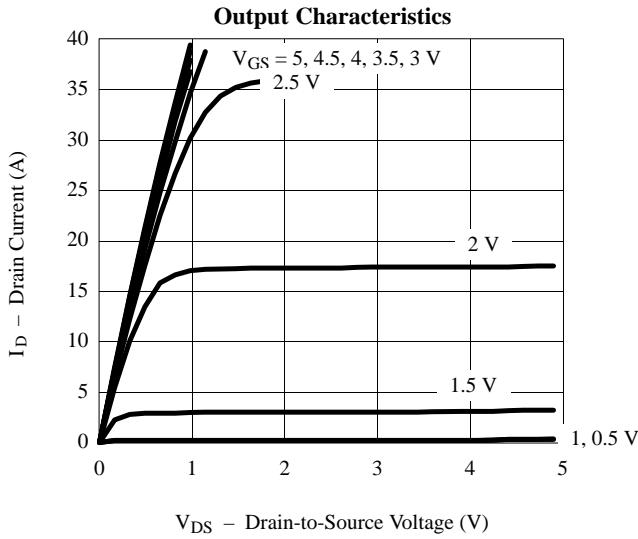
## Specifications ( $T_J = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>Static</b>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	0.6			V
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 8 \text{ V}$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 20 \text{ V}, V_{GS} = 0 \text{ V}$			1	$\mu\text{A}$
		$V_{DS} = 20 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 55^\circ\text{C}$			5	
On-State Drain Current <sup>a</sup>	$I_{D(on)}$	$V_{DS} \geq 5 \text{ V}, V_{GS} = 4.5 \text{ V}$	$\pm 20$			A
		$V_{DS} \geq 5 \text{ V}, V_{GS} = 2.5 \text{ V}$	$\pm 8$			
Drain-Source On-State Resistance <sup>a</sup>	$r_{DS(on)}$	$V_{GS} = 4.5 \text{ V}, I_D = 5.4 \text{ A}$		0.025	0.035	$\Omega$
		$V_{GS} = 2.5 \text{ V}, I_D = 4.9 \text{ A}$		0.030	0.04	
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = 10 \text{ V}, I_D = 5.4 \text{ A}$		22		S
Diode Forward Voltage <sup>a</sup>	$V_{SD}$	$I_S = 1.25 \text{ A}, V_{GS} = 0 \text{ V}$		0.7	1.2	V
<b>Dynamic<sup>b</sup></b>						
Total Gate Charge	$Q_g$	$V_{DS} = 6 \text{ V}, V_{GS} = 4.5 \text{ V}, I_D = 5.4 \text{ A}$		18	35	nC
Gate-Source Charge	$Q_{gs}$			2.5		
Gate-Drain Charge	$Q_{gd}$			4		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 6 \text{ V}, R_L = 6 \Omega$ $I_D \cong 1 \text{ A}, V_{GEN} = 4.5 \text{ V}, R_G = 6 \Omega$		35	60	ns
Rise Time	$t_r$			65	100	
Turn-Off Delay Time	$t_{d(off)}$			100	150	
Fall Time	$t_f$			33	60	
Source-Drain Reverse Recovery Time	$t_{rr}$	$I_F = 1.25 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$		50	100	

Notes

- a. Pulse test; pulse width  $\leq 300 \mu\text{s}$ , duty cycle  $\leq 2\%$ .  
b. Guaranteed by design, not subject to production testing.

**Typical Characteristics (25°C Unless Otherwise Noted)**



## Typical Characteristics (25°C Unless Otherwise Noted)

